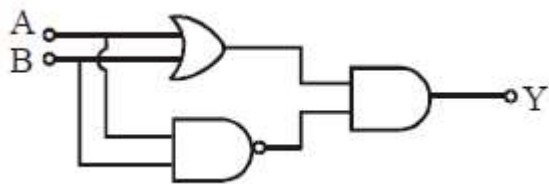


**U.G. 1st Semester Examination - 2021****COMPUTER SCIENCE****[HONOURS]****Course Code : COM.SC-H-CC-L-102****(Digital System Design)**

Full Marks : 60

Time :  $2\frac{1}{2}$  Hours*The figures in the right-hand margin indicate marks.**Candidates are required to give their answers in their own words as far as practicable.***GROUP-A**

1. Answer any **ten** questions:  $2 \times 10 = 20$
- Reduce  $AB + (AC)' + AB'C(AB + C)$ .
  - What is the basic difference between a counter and a shift register?
  - Solve for X when  $(137)_x = (5f)_{16}$ .
  - Define de-multiplexer.
  - State the output for the following circuit:



- Construct 3-8 decoder using 2-4 decoders. Block diagram is sufficient.
- Why race condition occurs in S-R flip-flop?
- What is the equivalent binary representation of the Gray coded no 10110?
- Define setup time.
- Define skew and clock skew.
- What is propagation delay?
- What is static hazard?
- Define noise margin.
- What are the advantages of CMOS logic over TTL logic family?

**GROUP-B**

- Answer any **four** questions:  $5 \times 4 = 20$
- Simplify the following equation using K-map to obtain minimum SOP equation and realize that using two level NAND gates only:  
 $F(A,B,C,D) = \Pi (1, 3, 4, 6, 9, 11, 12, 14)$
  - Design and implement Full subtractor using full adder.
  - Draw and explain the basic circuit of 4-bit DAC with the help of an example.

[Turn over]

5. Design a combinational circuit that multiplies two 2-bit binary values, and produces 4-bit product. Get the minterms for  $P_0$ ,  $P_1$ ,  $P_2$  and  $P_3$ . Simplify only  $P_2$ .
6. Design a synchronous J-K counter that goes through the following states:  
1, 3, 4, 5, 7, 1, 3,...
7. Explain how you can convert a D flip-flop into S-R flip-flop.

### GROUP-C

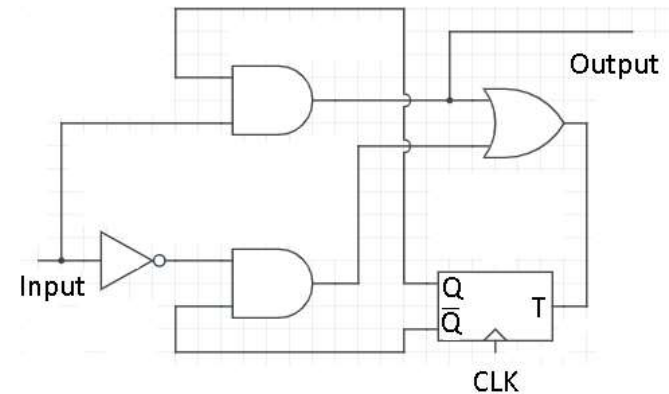
Answer any **two** questions: 10×2=20

8. a) Design a 4 to 2 priority encoder with 'valid' output where highest priority is given to the input with highest index and obtain minimal sum expressions for the outputs. Realize the expression with logic gates.  
b) Draw and explain how 3×8 decoder can be converted into 8 to 1 MUX. 6+4
9. a) What is Noise Margin?  
b) Implement the function  $F(A, B, C) = \sum m(1, 4, 5, 6)$  using 4 to 1 MUX and 2 to 1 MUX showing k-maps and logic circuits. 2+8
10. a) Design and explain the working of 4-bit ADDER/SUBTRACTOR circuit.

- b) Design a 3-bit odd parity generator circuit.

6+4

11. a) Analyse the following sequential circuit and obtain excitation table, transition equation, state table and transition diagram for the same.



- b) Realize 2 input X-OR gate using NOR gates only. 8+2